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Design and Simulation Analysis of a Symmetric 17-Level Multilevel Inverter Topology

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ABSTRACT: Multilevel inverters (MLIs) have gained significant attention in modern power electronics due to their ability to generate high-quality output voltages with reduced harmonic distortion. By synthesizing multiple voltage levels from several DC sources, MLIs offer improved performance in medium- and high-power applications compared to conventional two-level inverters. This paper proposes a symmetrical 17-level multilevel inverter topology designed to achieve enhanced voltage level generation while minimizing the number of power electronic components. The overall configuration is divided into two main sections: a level generation unit and a polarity reversal unit (H-bridge). The level generation stage produces the stepped voltage waveform, whereas the H-bridge enables full AC output by reversing the polarity. The proposed inverter employs twelve power switches, including bidirectional switches in the level generation stage, which allow flexible current conduction and proper insertion of DC sources. Operating in symmetrical mode with equal DC voltage sources, the topology generates fifteen distinct voltage levels, including the zero level, through appropriate switching combinations. A Carrier-Based Sinusoidal Pulse Width Modulation (CB-PWM) technique is implemented to control the switching operation and enhance the output waveform quality. The performance of the proposed inverter is validated through simulation analysis under RL load conditions. The results demonstrate that the inverter produces a high-quality staircase waveform with reduced total harmonic distortion (THD), improved voltage utilization, and efficient switching operation.

I. INTRODUCTION

Multilevel inverters (MLIs) have emerged as a crucial area of research in power electronics due to their wide range of applications and distinct technical benefits [1]–[5]. As global energy demand continues to rise, the integration of MLIs into advanced power conversion systems has become increasingly important [4], [5]. These inverters are commonly used in applications such as variable-frequency drives, electric vehicles, and high-voltage DC transmission systems [3], [4]. Additionally, they are essential in renewable energy systems, particularly in solar photovoltaic and wind energy conversion technologies [5]–[8]. Their ability to handle medium- and high-power levels makes them particularly suitable for high-voltage applications [4], [9]. One of the key features of MLIs is their capacity to produce high output voltages in stepped or staircase waveforms using multiple DC sources [1], [2]. This waveform closely resembles a sinusoidal shape, which significantly reduces total harmonic distortion (THD) and minimizes the need for large output filters [10]–[12]. Moreover, the reduced voltage change rate (dv/dt) alleviates stress on power switches and connected loads, thereby improving system reliability [13], [14]. Since each switching device experiences only a fraction of the total output voltage, components with lower voltage ratings can be used, contributing to a more cost-effective design [15]. Another notable advantage is the availability of multiple switching states to generate the same voltage level, introducing redundancy and enabling fault-tolerant operation [16]. Conventional MLI topologies include the Neutral-Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) configurations [1], [3], [17]. Although these designs offer substantial improvements over traditional two-level inverters, they often involve a large number of switches, capacitors, or isolated DC sources, leading to increased system complexity and cost [18], [19]. In response, researchers have developed new topologies aimed at reducing component count while preserving or improving performance [20]–[22]. Modern MLI structures are generally classified as symmetrical or asymmetrical based on the magnitudes of their DC sources [23]. Various modulation techniques have also been proposed to enhance output waveform quality and control performance [10], [24]. This paper introduces a symmetrical 17-level multilevel inverter (MLI) topology. The effectiveness of the proposed configuration is analyzed through MATLAB/Simulink simulations under RL load conditions at various modulation indices. The organization of the paper is structured as follows: Section 3 explains the operational principles and the modulation strategy adopted for the proposed inverter; Section 4 details the different operating states; and Section 5 outlines the simulation setup along with the corresponding results and discussion.

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II. PROPOSED TOPOLOGY

The structure of the proposed 17-level multilevel inverter (MLI) is shown in Fig. 1. The overall topology is composed of two main functional sections: the level generation unit and the polarity generation unit. In total, the circuit utilizes seventeen power semiconductor switches (S_1–S_{17}) along with eight DC voltage sources (V_1–V_8) to synthesize multiple voltage levels at the output. Among these switches, S_8, S_9, S_{12}, S_{13}, S_{16}, and S_{17} operate as bidirectional switches, allowing current to flow in both directions. This bidirectional conduction capability is important for achieving flexible voltage level generation and ensures proper current flow during different operating conditions. The remaining switches function as unidirectional switches, which are responsible for directing the current path according to the required switching state. The inverter is designed using a symmetrical configuration, where all the DC voltage sources have equal voltage magnitudes. This symmetrical arrangement provides several advantages, including balanced voltage stress across the switches, improved reliability, and simplified control and modulation strategies. The level generation unit is responsible for producing the stepped DC voltage levels required for multilevel operation. By selectively turning ON specific switches, the circuit either connects or bypasses the DC voltage sources in different series combinations, enabling the generation of multiple intermediate voltage levels. Through this switching mechanism, the inverter is capable of synthesizing seventeen distinct voltage levels at the output. The polarity generation unit is formed by four switches (S_1, S_2, S_3, and S_4) arranged in a full-bridge configuration. This section converts the generated stepped DC voltage from the level generation stage into both positive and negative half-cycles, thereby producing the required AC output waveform across the load. The combination of these two units enables the proposed topology to achieve high-quality output voltage with a larger number of levels while maintaining a relatively efficient circuit structure.

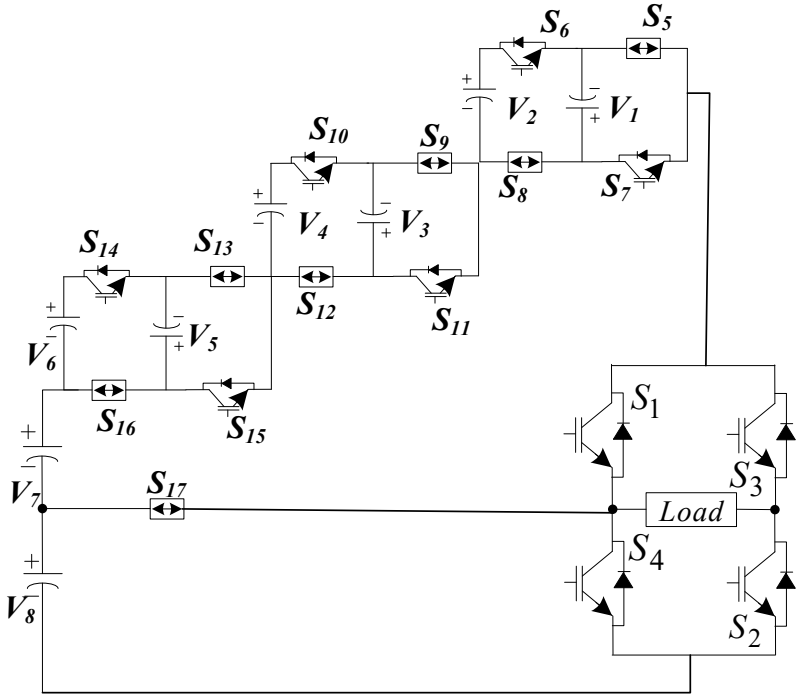

Fig. 1. Proposed MLI topology

III. MODULATION AND CONTROL OF MLI

In the 17-level multilevel inverter shown in Fig. 2(a), a low-frequency sinusoidal reference signal is compared with multiple high-frequency triangular carrier signals to generate the switching pulses. To obtain a 17-level output voltage, sixteen carrier signals are employed, each operating at a frequency of about 3 kHz. The sinusoidal reference signal sets the fundamental frequency of the inverter output, while its amplitude determines the modulation index, which controls the magnitude of the output voltage. Switching pulses are produced whenever the reference sinusoidal signal intersects with any of the carrier signals. As the reference signal moves across the different carrier bands, the inverter switches between several discrete voltage levels. This operation produces seventeen voltage levels, consisting of eight positive levels, eight negative levels, and one zero level.

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The switching sequence results in a staircase-type output waveform that closely approximates a sinusoidal waveform. Due to this multilevel structure, the total harmonic distortion (THD) is reduced, the dv/dt stress on the switching devices becomes lower, and the overall quality of the output voltage improves. The resulting stepped output voltage waveform obtained from this modulation technique is illustrated in Fig. 2(b).

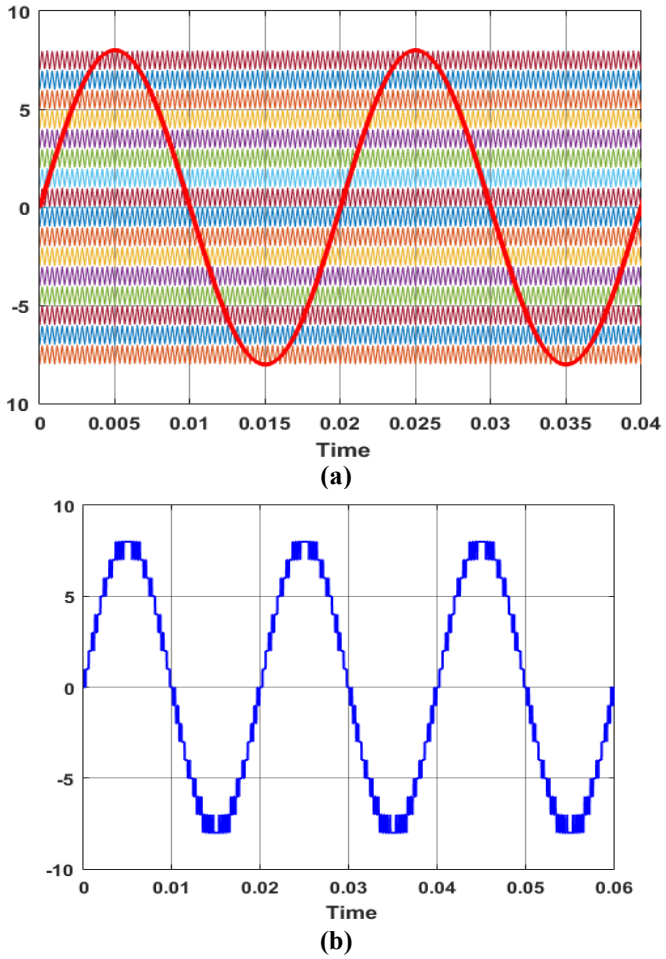

Fig. 2: Pulse-width modulation process: (a) Reference sine wave compared with carrier signals; (b) Generated switching waveform for the 17-level MLI.

IV. MODES OF OPERATION

The proposed multilevel inverter produces seventeen distinct voltage levels ranging from +8Vdc to −8Vdc by applying specific switching combinations, as summarized in Table 1. In the table, a check mark (√) denotes that the corresponding switch is ON, whereas a cross (×) indicates that the switch is OFF. During the positive half-cycle, the higher positive voltage levels are generated by properly connecting the DC sources through the switching network. The +8Vdc level is obtained when switches S1, S2, S6, S7, S10, S11, S14, and S15 are turned ON. The +7Vdc level is produced by activating S1, S2, S5, S6, S10, S11, S14, and S15. For the +6Vdc level, switches S1, S2, S7, S8, S10, S11, S14, and S15 conduct. The +5Vdc level is achieved by turning ON S1, S2, S9, S10, S14, and S15. Similarly, the intermediate voltage levels (+4Vdc, +3Vdc, +2Vdc, and +1Vdc) are generated through different combinations of switches mainly involving S1–S2 in the input stage and S14–S15 in the polarity generation unit, while the remaining switches selectively connect or bypass the DC sources to obtain the required stepped voltage magnitude. The zero-voltage state (0Vdc) is produced when the load terminals are isolated from the DC sources while maintaining a freewheeling path, which in this topology occurs when S2 and S4 are turned ON and the other switches remain OFF.For the negative half-cycle, the inverter generates the corresponding negative voltage levels (−1Vdc to −8Vdc) by reversing the current flow through the polarity generation unit. In this case, switches such as S3 and S4 replace S1 and S2 in the conduction path, while the remaining switches create the same source combinations used for the positive levels. Through these mirrored switching states, the inverter synthesizes −1Vdc, −2Vdc, −3Vdc, −4Vdc, −5Vdc,

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−6Vdc, −7Vdc, and −8Vdc. Overall, each of the seventeen voltage levels corresponds to a unique switching configuration, enabling the inverter to appropriately insert or bypass the available DC sources. This arrangement allows the converter to generate a stepped AC output waveform with improved resolution and reduced harmonic distortion. The corresponding switching modes and current conduction paths for these voltage levels are illustrated in Fig. 4, where the green arrows indicate the current path during the positive half-cycle, and the red arrows represent the conduction path during the negative half-cycle

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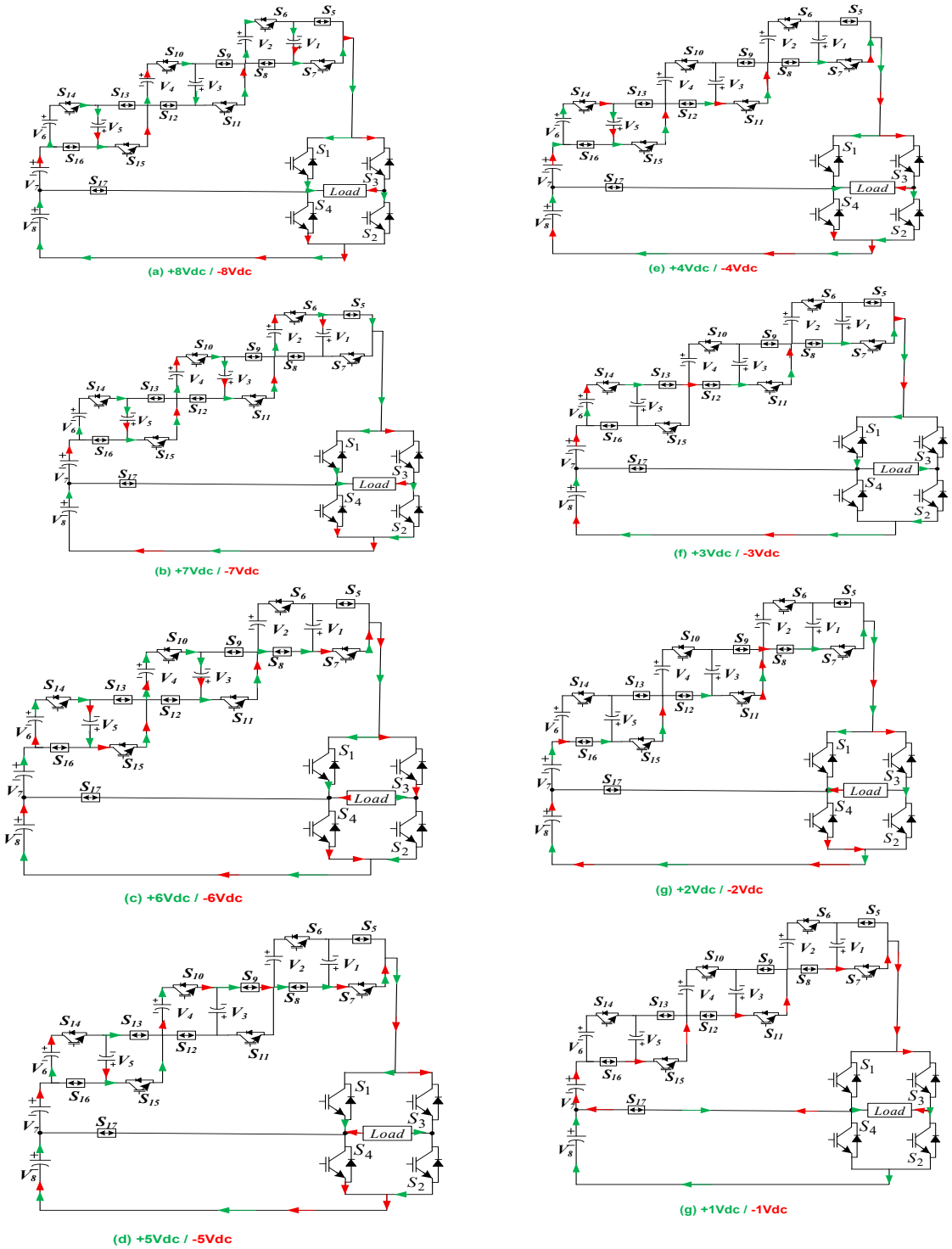

Fig.4. Modes of operation for positive and negative half cycle of the proposed MLI

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Table. 1. Switching status of proposed MLI

	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	S_{16}	S_{17}
$+8V_{dc}$	✓	✓	x	x	x	✓	✓	x	x	✓	✓	x	x	✓	✓	x	x
$+7V_{dc}$	✓	✓	x	x	✓	✓	x	x	x	✓	✓	x	x	✓	✓	x	x
$+6V_{dc}$	✓	✓	x	x	x	x	✓	✓	x	✓	✓	x	x	✓	✓	x	x
$+5V_{dc}$	✓	✓	x	x	x	x	x	x	✓	✓	x	x	x	✓	✓	x	x
$+4V_{dc}$	✓	✓	x	x	x	x	✓	✓	x	x	✓	✓	x	✓	✓	x	x
$+3V_{dc}$	✓	✓	x	x	x	x	✓	✓	x	x	✓	✓	✓	✓	x	x	x
$+2V_{dc}$	✓	✓	x	x	x	x	✓	✓	x	x	✓	✓	x	x	✓	✓	x
$+1V_{dc}$	x	✓	x	x	x	x	x	x	x	x	x	x	x	x	x	x	✓
$0V_{dc}$	x	✓	x	✓	x	x	x	x	x	x	x	x	x	x	x	x	x
$-1V_{dc}$	x	x	✓	x	x	x	✓	✓	x	x	✓	✓	x	x	✓	✓	✓
$-2V_{dc}$	x	x	✓	✓	x	x	✓	✓	x	x	✓	✓	x	x	✓	✓	x
$-3V_{dc}$	x	x	✓	✓	x	x	✓	✓	x	x	✓	✓	✓	✓	x	x	x
$-4V_{dc}$	x	x	✓	✓	x	x	✓	✓	x	x	✓	✓	x	✓	✓	x	x
$-5V_{dc}$	x	x	✓	✓	x	x	x	x	✓	✓	x	x	x	✓	✓	x	
$-6V_{dc}$	x	x	✓	✓	x	x	✓	✓	x	✓	✓	x	x	✓	✓	x	x
$-7V_{dc}$	x	x	✓	✓	✓	✓	x	x	x	✓	✓	x	x	✓	✓	x	x
$-8V_{dc}$	x	x	✓	✓	x	✓	✓	x	x	✓	✓	x	x	✓	✓	x	x

IV. SIMULATION AND EXPERIMENTAL RESULTS

This section presents the simulation results used to validate the performance of the proposed 17-level multilevel inverter (MLI) topology. A detailed simulation model of the system was developed using the MATLAB/Simulink R2019b platform. The inverter is designed with a symmetrical configuration that utilizes eight DC voltage sources of 30 V connected through the switching network to synthesize stepped voltage levels at the output. Since all the DC sources have identical voltage magnitudes, the inverter is capable of generating seventeen distinct voltage levels, ranging from the maximum positive level to the corresponding negative level with a zero state in between.

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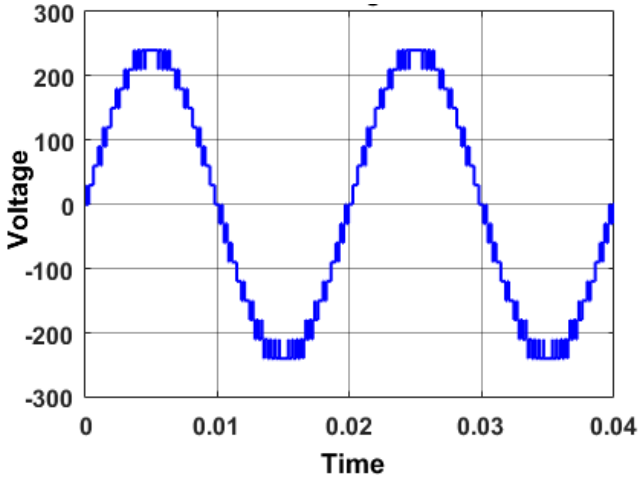
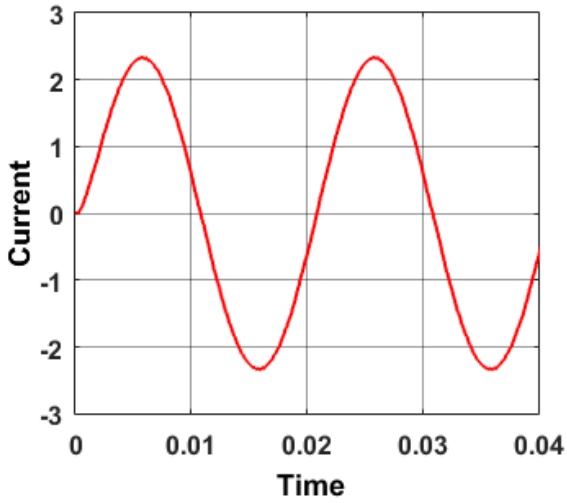
For performance analysis, the inverter was simulated at a modulation index of 1 while supplying an RL load consisting of a 100 Ω resistor connected in series with an 80 mH inductor. The simulation results show that the proposed topology successfully generates the required stepped output voltage waveform with improved quality. The inverter produces peak output voltage 240 V and the load current 2.35 A waveform follows the voltage profile with a peak value close to the designed operating range. These outcomes confirm the proper operation and effectiveness of the proposed 17-level inverter topology in producing multiple voltage levels with stable performance.



(a)



(b)

Fig. 4. Simulation results for the (a) output voltage; (b) load current; at MI = 1

V. CONCLUSION

A 17-level MLI topology is designed to generate a high-quality stepped AC output using a reduced and efficient circuit structure. The topology consists of two main sections: a level generation unit and a polarity generation unit. The inverter employs seventeen power switches and eight equal DC voltage sources, where several switches operate in bidirectional mode to provide flexible current flow and effective voltage level formation. The symmetrical configuration of the DC sources ensures balanced voltage stress across the switches and simplifies the overall control strategy. This arrangement enables the inverter to generate seventeen distinct voltage levels, which improves the output waveform quality and reduces harmonic distortion. To validate the performance of the proposed topology, a detailed simulation model was developed using MATLAB/Simulink R2019b. The inverter was tested under an RL load of 100 Ω and 80 mH at a modulation index of 1. The simulation results confirmed that the inverter successfully produces the expected stepped output voltage waveform with a peak output voltage of 240 V and a peak load current of approximately 2.35 A. These results demonstrate that the proposed topology operates effectively and is capable of

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generating multiple voltage levels with stable performance. Overall, the proposed 17-level MLI topology offers improved output waveform quality and reliable operation, making it a suitable candidate for applications requiring high-quality multilevel power conversion. Future work may include experimental validation and further analysis of harmonic performance and efficiency under different loading conditions.

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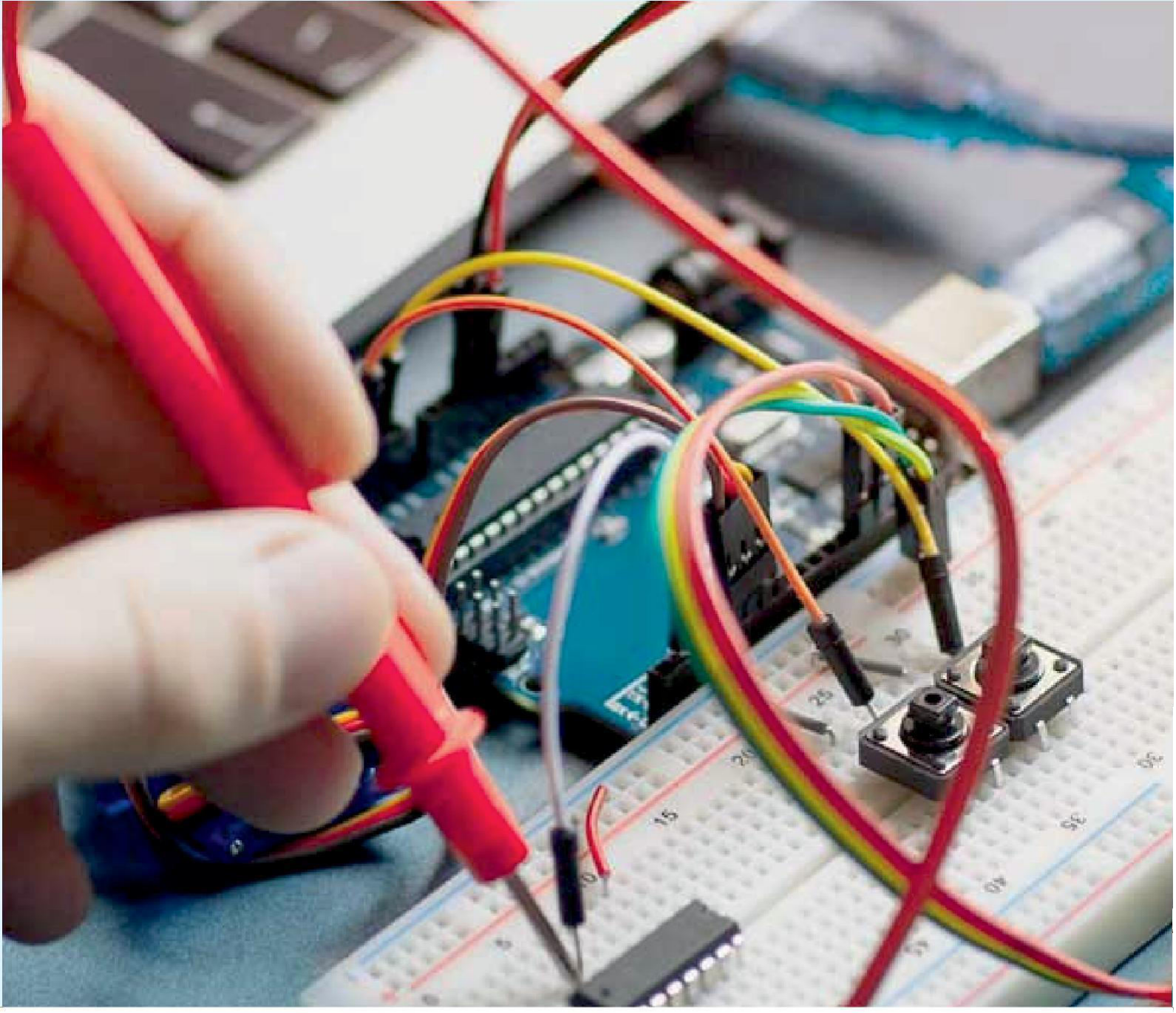

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